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(54) INFORMATION REPRODUCING DEVICE AND METHOD THEREFOR

(57) Abstract:

PROBLEM TO BE SOLVED: To detect a phase error of a PLL based on the state data by generating the state data expressing a maximum likelihood state transition in a viterbi decoding method.

SOLUTION: The state data as a series of a state data value expressing a state itself are generated by an SMU(status memory unit) 134 corresponding to the maximum likelihood state transition selected at every read clock by an ACS (selection circuit) 133 in a viterbi decoder 130. A timing generator 138 generates rising, falling timing of a regenerative RF signal from the state data. A PEC(phase error calculator) 137 generates a phase error signal PE based on a reproduction signal value (sampling value by A/D converter 12) sampled according to these timing, and uses the phase error signal PE for controlling a VCO(voltage control oscillator) 141. The memory length of the SMU 134 for generating the timing is made shorter than the memory length for decoding. This memory length is switchable also in a header area and a data area.